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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/542,783	04/04/2000	John Whitman	4294US(98-1208)	6870

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EXAMINER
KEBEDE, BROOK

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/542,783	Applicant(s) WHITMAN ET AL.
	Examiner Brook Kebede	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-87* is/are pending in the application.

4a) Of the above claim(s) *18-87* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *15* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on November 22, 2002 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 2, 8, 9, 11, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Kikuchi et al. (US/6,278,153).

Re claim l, Kikuchi et al. disclose a method for disposing a material on a semiconductor device structure comprising: providing a semiconductor device structure (see Fig. 6D) including

a surface (23 24 25 26) and at least one recess (23a) formed in the surface; disposing the material (20) on the surface (23 24 25 26) so as to substantially fill at least one recess (23a) and the material (20) covering the surface having a thickness less than a depth of said at least one recess (23a) without subsequently removing the material (20) from the surface, an upper surface of at least a portion of said material (20) over or within said at least one recess being substantially planar (23 24 25 26) (see Figs. 6A-6D; 10A-10E and 13A-13E;).

Re claim 2, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including disposing the material so as to substantially fill the at least one recess without substantially covering said surface (see Figs. 6A-6D; 10A-10E and 13A-13E;).

Re claim 8, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including upon exposing the material disposed over an entirety of said semiconductor device structure to an etchant, the material covering said surface is substantially removed therefrom, while the material located in said at least one recess substantially fills said at least one recess (see Figs. 6A-6D; 10A-10E and 13A-13E).

Re claim 9, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation wherein said providing said semiconductor device structure comprises providing a stacked capacitor structure with said at least one recess comprising at least one container formed in an insulator layer of said stacked capacitor structure, said surface and said at least one container being lined with a conductive material (see Figs. 6A-6D; 10A-10E; 13A-13E)

Re claim 11 as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a mask material over said semiconductor device structure (see Fig. 6A-6D; 10A-10E; 13A-13E).

Re claims 16 and 17, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation providing a semiconductor device structure having a surface with at least one dual damascene trench recessed therein and a layer of conductive material, with a non-planar surface disposed in said at least one dual damascene trench add at least partially covering sand surface and disposing a stress buffer over said layer of conductive material, said stress buffer having a substantially planar surface without removing material thereof following said disposing (see Figs. 14A-14D).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Yoshihara (US/6,117,486).

Re claims 3-7, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure (see Kikuchi et al. Figs. 6A-6D; 10A-10E and 13A-13E). However, Kikuchi et al. do not disclose decreasing a rate of the spinning while permitting the material to at least partially cure and gradually increasing the rate of the spinning.

Yoshihara discloses applying the material to the surface of the semiconductor device structure spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning; exposing the material to a soft balling temperature ; spinning rate of 1000 and 100 rpm (see Figs. 10 and Col. 13, lines 25-44). As Yoshihara discloses the method provided forming of resist film on the semiconductor wafer at predetermined and uniform thickness.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with spinning the semiconductor device structure both decreasing rate of spinning and while allowing the material to cure gradually increasing the rate of spinning as taught by Yoshihara because the method would have provided to form a resist film on the semiconductor wafer at predetermined and uniform thickness.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Lin et al. (US/6,046,083).

Re claim 10, as applied to claim 9 above, Kikuchi et al. disclose all the claimed limitations including forming of stacked capacitor structure having conductive layer. Although it is well-known in the art Kikuchi et al. do not disclose doped HSG.

Lin et al. disclose providing said semiconductor device structure having a stacked capacitor structure with the surface and at least one container being lined, with doped hemispherical grain polysilicon (see Figs. 7 and 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with doped HSG as taught by Lin et al. because the device performance would have been enhanced (see Lin et al. Col. 1, lines 59-67 through Col. 2, lines 1-14).

7. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (US/6,278,153) in view of Park et al. (US/6,326,282).

Re claim 12, as applied to claim 1 above, Kikuchi et al. disclose all the claimed limitations including the limitation except providing a shallow trench isolation structure with at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure.

Park et al. disclose forming of a shallow trench isolation structure with at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure in order to form an isolation region between the device elements (see Figs. 2B-2E).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Kikuchi et al. reference with

shallow trench isolation structure as taught by Park et al. because the shallow trench isolation structure would have provided isolation region between device elements in the substrate.

Re claim 13, as applied to claim 12 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a mask material over said shallow trench isolation structure (see Park et al. Figs. 2B-2E).

Re claim 14, as applied to claim 12 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said providing said shallow trench isolation structure comprises providing said shallow trench isolation structure with an insulator layer substantially filling said at least one trench and covering said surface see Park et al. Figs. 2B-2E).

Re claim 15, as applied to claim 14 above, both Kikuchi et al. and Park et al. in combination disclose all the claimed limitations including the limitation wherein said disposing the material comprises disposing a stress buffer over said insulator layer, said stress buffer having a substantially planar surface without removing material thereof following said disposing see Park et al. Figs. 2B-2E).

Response to Arguments

8. Applicants' arguments filed on October 15, 2002 in Paper No. 13 have been fully considered but they are not persuasive.

Regarding claim rejection of claims 1, 2, 8, 9, 11, 16, and 17 under 35 U.S.C. § 102(e) applicants argued that "Kikuchi falls to expressly or inherently describe teach a method for disposing a material on a semiconductor device structure over at least one recess, in which

method the material is disposed in such a way that at least the portion of the material located over or within the at least one recess has a substantially planar upper surface. Kikuchi shows, in Fig. 6D, an intermediate semiconductor device structure in which a layer of resist 20 that has been disposed within and over a via-hole 23a appears to have a planar surface. Kikuchi also discloses that the resist 20 can be applied by several methods known in the art, including spin-coating. Col. 17, lines 63-66. However, as pointed out by the "Background" section of the specification of the above-referenced application, at page 3, line 15, to page 4, line 29, the limitations in previously known spin-on methods, as well as material properties (e.g., surface tension, adherence to adjacent materials, etc.), prevent a layer of material, such as the resist disclosed by Kikuchi and illustrated in Fig. 6D, from having a substantially planar upper surface. As such, it is respectfully submitted that Kikuchi neither expressly nor inherently describes that resist 20 is disposed on a surface of a semiconductor device structure 21 such that the resist 20 over or within a via-hole 23 a thereof has an upper surface which is substantially planar…"

In response to the applicants' argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The rejected claims under 35 U.S.C. § 102(e) are anticipated by Kikuchi et al. '153 as applied in Paragraph No. 3 herein above. In addition, Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). Furthermore, the claims as recited in claim 1 does not specifically

call for a particular semiconductor device and the preamble recites "a method deposing a material on a semiconductor device structure comprising..." and the body of the claim also does not provide a positive or negative recitation that identified a particular semiconductor device. Therefore, applicants argument that Kikuchi et al. reference device has to be identical to instant application device has no merit since the recited claimed invention is within the scope of Kikuchi et al. '153, i.e., method of disposing a material on a semiconductor device structure is disclosed. Further, applicants' argument is so confusing because in one hand applicants arguing that Kikuchi et al. does not teach the claimed limitation on the other hand applicants are admittedly pointed out *"Kikuchi shows, in Fig. 6D, an intermediate semiconductor device structure in which a layer of resist 20 that has been disposed within and over a via-hole 23a appears to have a planar surface."* The Examiner respectfully submits that Kikuchi et al. teach all the claimed limitation including the limitation "an upper surface of at lest a portion of said material over or within said at lest one recess being substantially planar." And that also can be clearly seen in Fig. 6D of Kikuchi et al. reference. Therefore, the rejection under 35 U.S.C. § 102(e) is deemed proper.

Regarding claim rejection of claims 3-7under 35 U.S.C. § 103(a), applicants argued that "It is respectfully submitted that claims 3-7 are allowable, among other reasons, as depending either directly or indirectly from claim 1, which is itself allowable. Moreover, neither Kikuchi, Yoshihara, nor knowledge available to one ordinarily skilled in the art suggests the combination of the teachings of Kikuchi with Yoshihara to arrive at invention which is recited in claims 3-7. Kikuchi teaches that layers of resist may be spin-coated onto semiconductor substrates that include recesses. However, Kikuchi neither teaches or suggests that resist layers so formed have

substantially planar surfaces, at least over or within the recesses of such semiconductor substrates. Yoshihara teaches that by spinning a semiconductor wafer at high speeds ("as low as 2000 rpm" Col. 11, line 16), lowering the speed for a time, and re-increasing it to high speeds, the wafer can be coated with material in such a way that circular ripples do not appear thereon. Yoshihara does not, however, suggest that the techniques described therein are useful for disposing material within recesses such that the upper surface of at least the material within or over the recesses has a substantially planar upper surface. Accordingly, it is respectfully submitted that one of ordinary skill in the art would not have bee motivated to combine the teachings of Kikuchi and Yoshihara in the manner that has been asserted. Moreover, it appears that any motivation to combine the teachings of Kikuchi and Yoshihara could only have been improperly gleaned from the benefit of hindsight provided by the disclosure of the above-referenced application. For the above reason, the ordinarily skilled artisan would also likely consider the likelihood of success when combining Kikuchi and Yoshihara to be quite low."

In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The combination of Kikuchi et al. 153' and Yoshihara '486 as applied in Paragraph 7 herein above. Further, in response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392,

170 USPQ 209 (CCPA 1971). Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Regarding claim rejection of claim 10 under 35 U.S.C. § 103(a), applicants argued that "Claim 10 is allowable, among other reasons, as depending from claim 1, which is allowable."

In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The combination of Kikuchi et al. 153' and Lin et al '083 as applied in Paragraph 8 herein above.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Regarding claim rejection of claims 12-15, under 35 U.S.C. § 103(a), the applicants argued that "Claims 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of U.S. Patent 6,326,282 to Park et al. (hereinafter "Park"). It is respectfully submitted that claims 12-15 are allowable, among other reasons, as depending either directly or indirectly upon claim l, which is itself allowable and, thus, the arguments pertaining to claim 1 apply. Furthermore, the combination of references does not teach or suggest each and every element of either claim 14 or claim 15."

In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The combination of Kikuchi et al. 153' and Park et al. '282 as applied in Paragraph 7 herein above. In response to applicants' argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into

account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Conclusion

9. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
BK
December 13, 2002

Olik Chaudhuri
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